CLAIMS

1. In a multi-point communications system having a receiver and transmitter disposed at a primary site for communication with a plurality of remote service units disposed at respective secondary sites, the receiver of the primary site receiving OFDM/DMT signals over a number of transmission bins, a transmitter for use in one or more remote service units comprising:

first means for converting a signal into a first serial digital data stream;

second means for generating a second serial digital data stream from the first serial digital data stream of the first means, the second serial digital data stream being a digital representation of an OFDM/DMT signal that is to be transmitted to the receiver of the primary site, the second serial digital data stream being generated from the first serial digital data stream through a modulated direct digital synthesis thereof; and

third means for converting the second serial digital data stream into an analog OFDM/DMT signal for transmission to the receiver of the primary site.

2. A transmitter as claimed in claim 1 wherein the first means comprises a CODEC.

3. A transmitter as claimed in claim 1 wherein the first means comprises an analog-to-digital interface that generates a digital data output signal from an analog input signal.

4. A transmitter as claimed in claim 1 wherein the first means comprises a direct digital interface that generates a digital data output signal from a digital data input signal.

5. A transmitter as claimed in claim 1 wherein the first means comprises:

an analog-to-digital interface that generates a digital data output signal from an analog input signal;

a direct digital interface that generates a digital data output signal from a digital data input signal;

a data interface accepting the digital data output signal of the analog-to-digital interface and the digital data output of the direct digital interface to generate the first serial digital data stream.

6. A transmitter as claimed in claim 1 wherein the second means comprises:

an addressable sine table containing digital data corresponding to at least a portion of a sine wave, the sine table providing the digital data at an output thereof in response to address input signals;

control means, responsive to the first digital data stream, for generating the address input signals to the addressable sine table, multiplying the digital data output from the addressable sine table by a predetermined amplitude factor, and accumulating the amplified digital

data occurring over a single sample cycle to thereby generate individual data elements of the second digital data stream.

7. A transmitter as claimed in claim 6 wherein the control means comprises:

address control means for providing a sequence of addresses to the input of the addressable sine table to generate a sequence of digital data values at the output of the addressable sine table, the sequence of digital data values output from the addressable sine table corresponding to sine waves having frequency and phase characteristics corresponding to the frequency and phase characteristics of the OFDM/DMT signal that is to be transmitted to the receiver of the primary site;

amplitude control means for multiplying each digital data value output by the addressable sine table by a corresponding amplitude factor to generate the amplified digital data, the amplitude factor being dependent on the digital data of the first digital data stream; and

summing means for digitally summing the amplified digital data over the single sample cycle to generate an OFDM/DMT digital data value for each sample cycle.

8. A transmitter as claimed in claim 7 wherein the address control means comprises:

step-size means for controlling the step size of the sequence of addresses that are to be used to address the addressable sine table over a symbol period for a single transmission bin, the step size means comprising a plurality of step sizes, each step size respectively

corresponding to one of the bins that are to be transmitted to the receiver at the primary site;

phase control means for setting the start location at which the sine table is first addressed for each of the plurality of step sizes during a single symbol period, the phase control means being responsive to the digital data of the first digital data stream.

9. A transmitter as claimed in claim 8 wherein the plurality of step sizes correspond to a number of transmission bins less than the number of bins received by the receiver of the primary site.

10. A transmitter as claimed in claim 6 wherein the addressable sine table comprises digital data corresponding to a complete sine wave.

11. A transmitter as claimed in claim 9 wherein the addressable sine table comprises digital data corresponding to a complete sine wave.

12. A transmitter as claimed in claim 6 wherein the addressable sine table comprises digital data corresponding to a quarter sine wave.

13. A transmitter as claimed in claim 12 and further comprising an address modifier circuit disposed at the address input of the addressable sine table to facilitate generation of data representing a complete sine wave from the digital data in the addressable sine wave table.

14. An apparatus for accepting a serial data stream and generating a further serial data stream for subsequent digital-to-analog conversion to an OFDM/DMT signal, the apparatus comprising:

an addressable sine table containing digital data corresponding to at least a portion of a sine wave, the sine table providing the digital data at an output thereof in response to address input signals; and

a control circuit, responsive to the serial data stream, for generating the address input signals to the addressable sine table, and for multiplying the digital data output from the addressable sine table by a predetermined amplitude factor, and accumulating the amplified digital data occurring over a single sample cycle to thereby generate individual data elements of the further serial data stream.

15. An apparatus as claimed in claim 14 wherein the control circuit comprises:

an address control circuit for providing a sequence of addresses to the input of the addressable sine table to generate a sequence of digital data values at the output of the addressable sine table, the sequence of digital data values output from the addressable sine table corresponding to sine waves having frequency and phase characteristics corresponding to the frequency and phase characteristics of the OFDM/DMT signal; and

an amplitude control circuit for multiplying each digital data value output by the addressable sine table by a corresponding amplitude factor to generate the amplified digital data, the amplitude factor being dependent on the digital data of the digital data stream;

a summing circuit for digitally summing the amplified digital data over the single sample cycle to generate the individual data elements of the further serial data stream.

16. An apparatus as claimed in claim 15 wherein the plurality of step sizes correspond to a number of transmission bins less than the number of bins received by the receiver of the primary site.

17. An apparatus as claimed in claim 14 wherein the addressable sine table comprises digital data corresponding to a complete sine wave.

18. An apparatus as claimed in claim 15 wherein the addressable sine table comprises digital data corresponding to a complete sine wave.

19. An apparatus as claimed in claim 14 wherein the addressable sine table comprises digital data corresponding to a quarter sine wave.

20. An apparatus as claimed in claim 19 and further comprising an address modifier circuit disposed at the address input of the addressable sine table to facilitate generation of data representing a complete sine wave from the digital data in the addressable sine wave table.

21. In a multi-point communications system having a receiver and transmitter disposed at a primary site for communication with a plurality of remote service units disposed at respective secondary sites, the

receiver of the primary site receiving OFDM/DMT signals over a number of transmission bins, a transmitter for use in one or more remote service units comprising:

first means for converting a signal into a first serial digital data stream;

second means for generating a second serial digital data stream from the first serial digital data stream of the first means, the second serial digital data stream being a digital representation of an OFDM/DMT signal that is to be transmitted to the receiver of the primary site, the second serial digital data stream being generated from the first serial digital data stream;

a partial sequence filter accepting the second serial digital data stream and selectively filtering the second serial digital data stream to generate a partially filtered second serial digital data stream;

third means for converting the second partially filtered serial digital data stream into an analog OFDM/DMT signal for transmission to the receiver of the primary site.

22. A transmitter as claimed in claim 21 wherein the second serial digital data stream is generated from the first serial digital data stream by direct digital synthesis of the first serial digital data stream.

23. A transmitter as claimed in claim 21 wherein the partial sequence filter comprises:

a FIR filter having an input and an output;

bypass control means for selectively supplying first and second subsets of digital data of the second serial digital data stream to the input of the FIR filter and for bypassing a third subset of digital data of the second serial digital data stream around the FIR filter to an output, the first subset of digital data representing the beginning portion of an OFDM/DMT symbol, the second subset of digital data representing the end portion of the OFDM/DMT symbol, and the third subset of digital data representing the mid portion of the OFDM/DMT symbol; and

selection means for selectively providing either the output of the FIR filter or the output of the bypass control means to the third means as the second partially filtered digital data stream.

24. A transmitter as claimed in claim 23 wherein the FIR filter comprises 101 taps.

25. A transmitter as claimed in claim 23 wherein the FIR filter is a symmetric filter.

26. A partial sequence filter for filtering a digital data stream representing a plurality of symbols of an OFDM/DMT transmission, the partial sequence filter comprising:

a FIR filter having an input and an output;

bypass control means for selectively supplying first and second subsets of digital data of the digital data stream to the input of the FIR filter and for bypassing third subsets of digital data of the digital data stream around the FIR filter to an output, the first subsets of digital data

representing the beginning portions of the OFDM/DMT symbols, the second subsets of digital data representing the end portions of the OFDM/DMT symbols, and the third subsets of digital data representing the mid portions of the OFDM/DMT symbols; and

selection means for selectively providing either the output of the FIR filter or the output of the bypass control means as an output of the partial sequence filter.

27. A partial sequence filter as claimed in claim 26 wherein the FIR filter comprises 101 taps.

28. A partial sequence filter as claimed in claim 26 wherein the FIR filter is a symmetric filter.

29. A partial sequence filter as claimed in claim 26 wherein the FIR filter comprises:

a first symbol data register having an input for receiving individual data samples of the digital data stream and an output;

a second symbol data register having an input for receiving individual data samples of the digital data stream and an output;

an adder connected to receive the outputs of the first and second symbol data registers to provide an output sum of the data samples contained therein;

a coefficient table memory for storing and selectively supplying tap coefficients corresponding to the desired filter characteristics of the FIR filter at an output thereof;

a multiplier circuit connected to receive the output sum from the adder and to receive the output of the coefficient table memory, the multiplier circuit multiplying the output sum by a data value at the output of the coefficient table memory to generate a multiplied data value;

an accumulator for summing the multiplied data values output from the multiplier circuit to generate filtered data samples; and

an output buffer connected to store the filtered data samples.

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